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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/753,262	01/05/2004	Simon Joshua Waters	1011-67363	6703

7590 02/14/2007

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EXAMINER	
LEVIN, NAUM B	
ART UNIT	**PAPER NUMBER**
2825	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/14/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/753,262	WATERS ET AL.	
	Examiner	Art Unit	
	Naum B. Levin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 September 2006 and 13 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *41-87* is/are pending in the application.

4a) Of the above claim(s) *41-50,63-71 and 75-87* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *51-62 and 72-74* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/753,262, Amendment filed on 09/15/2006 and Response to election/restriction filed on 12/13/2006.

2. Applicant has provisionally elected claims 51-62 and 72-74 (Group 2) with traverse. Claims 41-50, 69-71 and 79-83 (Group 1) and claims 63-68, 75-78 and 84-87 (Group 3) are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected. Applicant timely traversed the restriction (election) requirement in the reply filed on 10/31/2006.

3. The possible inventions of Group 1 (claims 41-50, 69-71 and 79-83), Group 2 (claims 51-62 and 72-74) and Group 3 (claims 63-68, 75-78 and 84-87) related to program/method/system of transforming a programming language specification into a lower-level specification, but Group 2 includes additional utilities, such as:" the programming language specification **including plural calls to plural instances of a unit class, wherein calls map to instances", "the programming language specification lacks explicit concurrency modeling** for the plural instances of the unit class", " **transforming includes generating lower-level description for handling concurrent execution of units** represented by the plural instances of the unit class in the programming language specification".

Applicant's Specification also distinguishes these groups such as: "According to a third aspect of the design approach ... the design tool interprets an interface in a programming language specification as specifying a design unit interface in HDL. Or, based upon structural relationships implied in the programming language specification,

the design tool generates code for handling sub-design unit concurrency and synchronization – page 4, ll.6-17".

Group 3 also includes additional utilities, such as: "**performing algorithmic simulation with executable produced by a compiling**".

Applicant's Specification also distinguishes these groups such as: "According to a second aspect of the design ... The design approach also enables simulation of a programming language specification with pre-existing specifications - page 3, ll.29-30, page 4, ll.1-5".

As such, the restriction is hereby made final.

4. Examiner finds Applicant's comments persuasive on the application of Schaumont on the claims. However, the newly sited reference reads on the claims as presently written.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

5. Claim 58 is rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The claimed invention lacks patentable utility.

The terms "a design input module for accepting an algorithmic specification"; "a hardware description language transformer for transforming the algorithmic specification into a lower-level specification" in the claim do not show any functional descriptive materials for getting the utility output, therefore they are missing the patentable utilities.

The claims appear to use functions or definitions without providing a useful, concrete and tangible result.

Specification

6. The disclosure is objected to because of the following informalities: the cross-reference information must be updated in "Amendments to the Specification" filed on 01/05/2004.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 51-62 and 72-74 are rejected under 35 U.S.C. 102(e) as being unpatentable by Panchul et al. (US Patent 6,226,776).

8. As to claims 51, 58 and 72 Panchul discloses:

(51) A computer readable medium storing computer executable instructions for causing a computer system programmed thereby to perform a method of transforming a programming language specification into a lower-level specification, the method comprising (col.5, ll.37-46; col.11, ll.63-67; col.12, ll.1-10):

accepting a programming language specification (statements in ANSI C high-level programming language used to render hardware designs vary – col.14, ll.49-50), the programming language specification including plural calls to plural instances of a unit class (various ANSI C functions can be classified "simple expression functions," such as "func1" and "func2" shown in FIG. 3A : (int func1, int funct2 mean initiate classified functions and correspond to calls of unit class)– col.14, ll.51-53), wherein a first call of the plural calls maps to a first instance of the plural instances of the unit class, wherein a second call of the plural calls maps to a second instance of the plural instances of the unit class (FIG. 3A illustrates C-type programming language expressions "a+b c<<3" and "(a b) & c". In these expressions, "a", "b", and "c" are integer variables. FIG. 3B illustrates that these expressions are mapped into RTL Verilog expressions "((param_func1_a+param_func1_b) (param_func1_c <<16'd3))" and "((param_func2_a param_func2_b) & param_func2_c)", respectively. Also, integer variables "a", "b", and "c" in FIG. 3A are mapped onto wires "param_func1_a", "param_func1_b", and "param_func1_c" for ANSI C function "func1" and wires "param_func2_a", "param_func2_b", and "param_func2_c" for ANSI C function "func2", respectively. This is because the ANSI C functions "func1" and "func2" are simple C-type functions – col.14, ll.66-67; col.15, ll.1-9), and wherein the programming language specification lacks explicit concurrency modeling for the plural instances of the unit class (FIGS. 3A and 3B also illustrate a plurality of selected C-type functions that can execute simultaneously, ... The determination of whether or not a plurality of simultaneously executable C-type functions is present is performed by the code shown

in the source code listing which appears in microfiche Appendix A in file OSYMBOLS.CPP at lines 5052-5232 – col.15, ll.31-38) (col.14, ll.49-67; col.15, ll.1-43); and

transforming the programming language specification into a lower-level specification, wherein the transforming includes generating lower-level description for handling concurrent execution of units represented by the plural instances of the unit class in the programming language specification (the invention comprises mapping predetermined C-type programming language expressions to functionally equivalent HDL program language expressions. FIG. 3A illustrates a simple expression function in ANSI C programming language, and FIG. 3B represents the function shown in FIG. 3A compiled into RTL Verilog HDL – col.14, ll.42-48; FIGS. 3A and 3B also illustrate a plurality of selected C-type functions that can execute simultaneously, which are compiled into a plurality of executable HDL program language expressions that operate in parallel ... Compilation of the plurality of simultaneously executable C-type functions to a plurality of HDL expressions that operate in parallel is performed by the code shown in the source code listing which appears in microfiche Appendix A in file GCODE.CPP at lines 5889-5990 - col.15, ll.31-43) (Abstract; Fig. 2; col.14, ll.42-48; col.15, ll.31-43);

(58) A design tool comprising (col.5, ll.37-46; col.11, ll.63-67; col.12, ll.1-10):

a design input module for accepting an algorithmic specification, the algorithmic specification including plural unit calls that map to plural different instances of a unit,

thereby indicating parallel execution of the plural unit calls (col.14, ll.49-67; col.15, ll.1-43); and

a hardware description language transformer for transforming the algorithmic specification into a lower-level specification, wherein the transformer adds code into the lower-level specification (the preliminary hardware design is compiled into a hardware description language (HDL) synthesizable design, as indicated by the step 40 (C to HDL Compiler) shown in FIG. 2. For example, the C-type programming language preliminary hardware design can be compiled into to a Verilog synthesizable design to produce an RTL hardware design file 42 – col.13, ll.34-37) for handling the parallel execution of the plural unit calls (Abstract; Fig. 2; col.13, ll. 30-43; col.14, ll.42-48; col.15, ll.31-43);

(72) In a computing environment, a computer-implemented method of transforming a programming language specification into a lower-level specification, the method comprising (col.5, ll.37-46; col.11, ll.63-67; col.12, ll.1-10):

providing a programming language specification, the programming language specification including plural unit calls that map to plural different instances of a unit class, thereby indicating parallel execution of the plural unit calls (Fig. 2; col.14, ll.49-67; col.15, ll.1-43); and

receiving a lower-level specification produced by transforming the programming language specification into the lower-level specification, wherein the transforming includes adding code into the lower-level specification for handling the parallel execution of the plural unit calls (Abstract; Fig. 2; col.13, ll. 30-43; col.14, ll.42-48; col.15, ll.31-43);

9. As to claims 52-57, 59-62 and 73-74 Panchul recites:

(52), (53) The computer readable medium, wherein the method further comprises transforming into a synchronized process of the lower-level specification (col.5, ll.14-35; col.6, ll.6-22);

(54)) The computer readable medium, wherein transforming includes transforming each input/output method into an input/output port of the port map (col.5, ll.29-36; col.5, ll.47-55);

(55) The computer readable medium/tool, wherein the programming language specification includes an object-oriented class description (col.6, ll.23-42);

(56)-(57), (61)-(62) A file including the programming language specification, a file including the lower-level specification (col.13, ll.1-11; col.13, ll.30-43; Fig.2);

(59) The design tool further comprising an architecture exploration module for presenting alternative architectures (col.13, ll.24-28);

(60) The design tool, wherein the unit is a sub-design unit (col.14, ll.42-67; col.15, ll.1-43);

(73) The method, the programming language specification is provided to one or more transformer modules (col.7, ll.59-64);

(74) The method, wherein the computing environment is a distributed computing environment (col.11, ll.54-62).

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

10. Claims 51, 58 and 72 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 9, 14 and 14 accordingly of U.S. Patent No. 6, 701,501. Independent claim 51 in the Application is similar to claim 9 in the reference because it recites various scope of invention.

Claims 51, 58 and 72 in the application disclose a computer readable medium storing computer executable instructions for causing a computer system programmed thereby to perform a method of transforming a programming language specification into a lower-level specification, the method comprising: accepting a programming language specification, the programming language specification including plural calls to plural instances of a unit class, wherein a first call of the plural calls maps to a first instance of the plural instances of the unit class, wherein a second call of the plural calls maps to a second instance of the plural instances of the unit class, and wherein the programming language specification lacks explicit concurrency modeling for the plural instances of the unit class; and transforming the programming language specification into a lower-level specification, wherein the transforming includes generating lower-level description for

handling concurrent execution of units represented by the plural instances of the unit class in the programming language specification. Claims 9 and 14 in the reference recite similar computer readable medium to perform a method that includes all above limitations plus following additional limitations: "accepting a programming language specification **for a design unit**".

Although the conflicting claims are not identical, they are not patentably distinct from each other because it would have been obvious to a person of ordinary skills in the art to use the computer readable medium storing computer executable instructions for causing a computer system programmed thereby to perform a method of transforming a programming language specification into a lower-level specification, the method comprising: accepting a programming language specification, the programming language specification including plural calls to plural instances of a unit class, wherein a first call of the plural calls maps to a first instance of the plural instances of the unit class, wherein a second call of the plural calls maps to a second instance of the plural instances of the unit class, and wherein the programming language specification lacks explicit concurrency modeling for the plural instances of the unit class; and transforming the programming language specification into a lower-level specification, wherein the transforming includes generating lower-level description for handling concurrent execution of units represented by the plural instances of the unit class in the programming language specification for implementing it in the computer readable medium to perform the method described in U.S. Patent 6, 701,501.

For example, it would have been obvious to the computer readable medium storing computer executable instructions for causing a computer system programmed thereby to perform a method of transforming a programming language specification into a lower-level specification, comprising: "accepting a programming language specification **for a design unit**".

Independent claims 51, 58 and 72 in the Application are similar to claims 9, 14, and 14 respectively in the reference because they recite various scope of invention in the same way as described above.

Dependent claims 52-57, 59-62 and 73-74 in the application are similar to claims 10-13, 15-16, 20, 21, 29-31 and 34 in the reference because they recite various scope of invention.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naum B. Levin whose telephone number is 571-272-1898. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

N L

JACK CHIANG
SUPERVISORY PATENT EXAMINER